DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's submission of the Appeal Brief filed on March 14, 2008 is acknowledged. Applicant's remarks submitted in the Appeal Brief are considered persuasive. In view of the Appeal Brief filed on March 14, 2008, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Therefore the FINALITY of the office action dated December 11, 2007 is hereby withdrawn. The examiner requests the applicants to consider the new grounds of rejection provided below. Currently, claims 2-3, 20-21 and 33-34 are canceled and claims 1, 4-19, 22-32 and 35-43 are pending for examination.

I. OBJECTION TO ABSTRACT

2. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because the abstract disclosure is insufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. Correction is required. See MPEP § 608.01(b).

II. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4, 6-14, 18-19, 22-32 and 35-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya et al. (US Pub.: 2003/0131166), Ooi et al. (US Patent 6,854,045) and Ooi et al. (US Patent 6,961,787).

6. As per claims 1, 18 and 31, Grieff teaches a switch coupled between a plurality of host units and a device via serial advanced technology attachment (SATA) for communicating there between and said switch comprising:

a) a first SATA port (Fig. 1, ref. 130) for connection to a first host unit, said first port for causing access, to the device, by the first host unit (col. 3, ll. 13-24 and col. 5, l.17 to col. 7, l. 6);

b) a second SATA port (Fig. 1, ref. 132) for connection to a second host unit, said second port for causing access to the device, by the second host unit (col. 3, ll. 13-24 and col. 5, l.17 to col. 7, l. 6);

c) a third SATA port (device-side link layer on Fig. 1) for connection to a device, for causing access to the device, by the first or second host units (col. 3, ll. 13-24 and col. 5, l.17 to col. 7, l. 6);

d) an arbitration and control circuit (arbiter module 112 and switch 110 of Fig. 1), coupled to the first, second and third ports, for selecting one of the first host unit or the second host unit to be coupled to the device, through the switch (col. 3, ll. 13-24 and col. 5, l.17 to col. 7, l. 6); and

wherein the switch enable multiple hosts to share access to the device (e.g. single ATA device) (col. 3, ll. 14-16), such that the device can maintain communication with the multiple hosts (col. 3, ll. 43-45); and

wherein the switch includes a buffer that allows the first host to post a single, non-queue command if the second host currently has outstanding queued commands (col. 5, ll. 36-39).

Grieff does not expressly teach the switch comprising:

wherein the first SATA port includes a first host task file that is responsive to commands sent by the first host unit;

wherein the second SATA port includes a second host task file that is responsive to commands sent by the second host unit;

wherein the third port is a PATA port;

selecting one of the first host or the second host units to concurrently access the device by accepting commands, from either of the first or the second host units, at any given time, including when the deice is not in an idle state.

"SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA" teaches the utilization of PATA ("SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", pages 1-2).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA's utilization of the PATA into Grieff's switch for the benefit of having a peripheral port that is backward comparable allowing users to be able to connecting existing PATA peripheral devices instead of purchasing new peripheral devices that conform to the new SATA standard to obtain the invention as specified in claims 1, 18 and 31. The resulting combination of the references teaches the switch comprising of a third PATA port connecting to a peripheral device.

Utsunomiya teaches a system and a method comprising:

a host computer issuing a plurality of commands to the drive apparatus (Fig. 3, ref. 12) at the same time (e.g. concurrently), wherein the drive apparatus operates in accordance to ATA ([0004] and [0007]);

a command queue including a task file queue enabling the host computer to issue the plurality of commands to be processed by the drive apparatus at the same time (e.g. concurrently), as the task file queue storing the plurality of commands ([0005]-

[0008] and [0020]-[0024]), therefore the task file queue would enable the host computer to issue the plurality of commands, at any given time, even when the drive apparatus is in a busy status ([0005]); and

wherein the plurality of commands issued by the host computer are transferred from the task file queue to the drive apparatus' task file (Fig. 5 and [0022]).

Ooi ('045) teaches a system and a method comprising a SATA port (Fig. 2, ref. 220, 230) having a serial port task file (Fig. 2, ref. 225, 235) (col. 3, l. 56 to col. 5, l. 15).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Utsunomiya and Ooi's task file queue into Grieff and SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA's ATA ports for the benefit of decreasing the work load of the host unit for issuing commands (Utsunomiya, [0009]) and provide backward compatibility between SATA and PATA (Ooi ('045), col. 1, ll. 13-42) to obtain the invention as specified in claims 1, 18 and 31; additionally, the combining of the above references would be motivated because it is well known to one skilled in the art for ATA that SATA specification provides for systems having forward and backward compatibility with PATA as well as scalability and evolutionary enhancement to various types of computing platforms and chipsets in computer systems (Ooi ('787), col. 1, ll. 13-42). The resulting combination of the references further teaches the switch comprising:

wherein the first SATA port includes the first task file queue (i.e. first host task file) storing the plurality of commands issued and sent by the first host unit;

wherein the second SATA port includes the second task file queue (i.e. second host task file) storing the plurality of commands issued and sent by the second host unit; and

wherein the switch selects either the first host unit or the second host unit to concurrently access the drive apparatus (i.e. device) as the switch receives and accepts the plurality of commands, issued by either the first host unit or the second host unit, at any give time, including when the device is in the busy status (i.e. not in an idle state), as the plurality of commands are respectively stored into the first task file queue and the second task file queue.

7. As per claims 4, 22 and 35, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi teach all the limitation of claims 1, 18 and 31 as discussed above, where Utsunomiya further teaches the switch comprising wherein said third parallel ATA port includes a device task file (Utsunomiya, Fig. 5 and [0022]).

8. As per claims 6, 23 and 36, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi teach all the limitation of claims 1, 18 and 31 as discussed above, where Grieff further teaches the switch comprising wherein said device is a storage unit (Grieff, col. 15, ll. 9-22).

9. As per claims 7, 24 and 37, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi teach all the limitation of claims 1, 18 and 31 as discussed above, where Grieff further teaches the switch comprising wherein said switch is employed in an enterprise system (Grieff, col. 15, ll. 9-22).

10. As per claims 8, 25 and 38, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi teach all the limitation of claims 1, 18 and 31 as discussed above, where Utsunomiya further teaches the switch wherein said arbitration and control circuit causes concurrent access of the device by the first and second host units (Utsunomiya, [0007] and [0020]-[0024]).

11. As per claims 9, 26 and 39, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi teach all the limitation of claims 1, 18 and 31 as discussed above, where Grieff further teaches the switch comprising wherein information, in the form of data, commands or setup, is transferred from the device to the first or second host units through the switch and the information is modified by the switch prior to being received by the first or second host units such that modified information rather than the information is received by the first or second host units (Grieff, col. 12, l. 60 to col. 14, l. 28).

12. As per claims 10, 27 and 40, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi teach all the limitation of claims 9, 26

and 39 as discussed above, where Grieff further teaches the switch comprising wherein the information is referred to as `identify drive response` (IDENTIFY DEVICE) (Grieff, col. 7, ll. 39-61).

13. As per claims 11, 28 and 41, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi teach all the limitation of claims 9, 26 and 39 as discussed above, where Grieff further teaches the switch comprising wherein the information is referred to as `Tag` (Grieff, col. 12, l. 60 to col. 14, l. 28).

14. As per claims 12, 29 and 42, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi teach all the limitation of claims 1, 18 and 31 as discussed above, where Grieff further teaches the switch comprising wherein information, in the form of data, commands or setup, is transferred from the first or second host units to the device through the switch and the information is modified by the switch prior to being received by the device such that modified information rather than the information is received by the device (Grieff, col. 5, l. 65 to col. 6, l. 56 and col. 10, l. 27 to col. 11, l. 36).

15. As per claims 13 and 43, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi teach all the limitation of claims 12 and 42 as discussed above, where Grieff further teaches the switch comprising wherein the

information is referred to as `Tag` (Grieff, col. 5, l. 65 to col. 6, l. 56 and col. 10, l. 27 to col. 11, l. 36).

16. As per claim 14, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi teach all the limitation of claim 13 as discussed above, where Grieff further teaches the switch comprising wherein the arbitration and control circuit include a Tag/Sactive Mapping Circuit (Grieff, Command Tracker SM 114 of Fig. 1) for mapping the host tag to the device tag and inverse mapping for identifying a host (Grieff, col. 5, l. 65 to col. 6, l. 56; col. 10, l. 27 to col. 11, l. 36 and col. 12, l. 60 to col. 14, l. 28).

17. As per claims 19 and 32, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi teach all the limitation of claims 18 and 31 as discussed above, where Grieff further teaches the switch comprising wherein the switch is a serial ATA switch (Grieff, col. 3, l. 13 to col. 4, l. 4 and col. 5, l. 65 to col. 6, l. 56).

18. As per claim 30, Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi teach all the limitation of claim 28 as discussed above, where Grieff further teaches the switch comprising wherein the information is referred to as `Tag` (Grieff, col. 5, l. 65 to col. 6, l. 56 and col. 10, l. 27 to col. 11, l. 36).

19. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813), "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya et al. (US Pub.: 2003/0131166), Ooi et al. (US Patent 6,854,045) and Ooi et al. (US Patent 6,961,787) as applied to claims 1, 4, 6-14 and 18-43 above, and further in view of Boucher et al. (US Patent 6,434,620).

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi teach all the limitations of claim 4 as discussed above, where Utsunomiya further teaches the switch comprising wherein said first, second and third ports include the corresponding task file queue (Fig. 4-5 and [0020]-[0024]).

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi do not expressly teach the switch comprising wherein said first, second and third ports are level 4 ports.

Boucher teaches a communication interface between a peripheral comprising the intelligent network interface card (INIC 50 of Fig. 1) and a host (Fig. 1, ref. 52) comprising a physical layer communication path (Fig. 1, ref. 57) and two other communication paths at higher communication layer (Fig. 1 and col. 6, l. 60 to col. 7, l. 10).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Boucher's higher layer communication path into Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi's switch for the benefit of providing a faster communication path between the peripheral device and the host (Boucher, Fig. 1) to obtain the invention as specified in

claim 5. The resulting combination of the references teaches the switch further comprising the ports, interconnection between the hosts and the peripheral device, operating at level 4, as it is well known to one skilled in the art that the highest communication layer for SATA is application layer (level 4).

20. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya et al. (US Pub.: 2003/0131166), Ooi et al. (US Patent 6,854,045) and Ooi et al. (US Patent 6,961,787) as applied to claims 1, 4, 6-14 and 18-43 above, and further in view of "Serial ATA Specification".

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi teach all the limitations of claim 1 as discussed above; but Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi do not expressly teach the switch comprising wherein either the first or the second host sends a legacy queue command queued by the device; and wherein either the first or the second host sends a native queue command for execution thereof by the device.

"Serial ATA Specification" teaches the utilization of the legacy ATA queuing (legacy queue command) and the native Serial ATA queuing (native queue command) by the Serial ATA device (Section D.1.5 on page 301).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Serial ATA Specification's queuing of legacy queuing command and the execution of the native queuing command into Grieff, "SATA vs.

PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi's switch because Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi's storage device conforms to the Serial ATA standard, therefore it would be beneficial to comply with the SATA standard in order to enable proper technological functioning in accordance with the SATA standard to obtain the invention as specified in claims 15-16.

21. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya et al. (US Pub.: 2003/0131166), Ooi et al. (US Patent 6,854,045) and Ooi et al. (US Patent 6,961,787) as applied to claims 1, 4, 6-14 and 18-43 above, and further in view of Shin et al. (US Patent 7,154,905).

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi teach all the limitations of claim 1 as discussed above, where Grieff further teaches the switch comprising:

wherein said first, second and third ports are operating at link layer (level 2 ports) (Grieff, Fig. 1); and

a Data FIS FIFO (Grieff, host FIS buffer 120 and device FIS buffer 122 of Fig. 1) and an associated FIFO Control (Grieff, Command Tracker SM 114 of Fig. 1) are coupled to the first, second and third ports and are located externally thereto (Grieff, Fig. 1 and col. 5, l. 65 to col. 6, l. 56).

Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi do not expressly teach the switch comprising wherein the first, second and third ports are level 3 SATA ports.

Shin teaches the utilization of a port including a transport layer (i.e. level 3 serial ATA port) (Fig. 1; Fig. 38A and col. 2, ll. 26-44).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Shin's transport layer into Grieff, "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya and Ooi's ATA ports for the benefit of providing a communication architecture that provides high-performance for applications at a low cost (Shin, col. 4, ll. 25-30) to obtain the invention as specified in claim 17. The resulting combination of the references teaches the switch coupled between the plurality of host units, further comprising wherein the first, second and third ports are level 3 serial ATA ports.

III. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1, 4-19, 22-32 and 35-43 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

April 09, 2008

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2163